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Challenges in Interconnection Design for LSI Chips and the Crucial Task of Developing a Suitable Design Automation Tool

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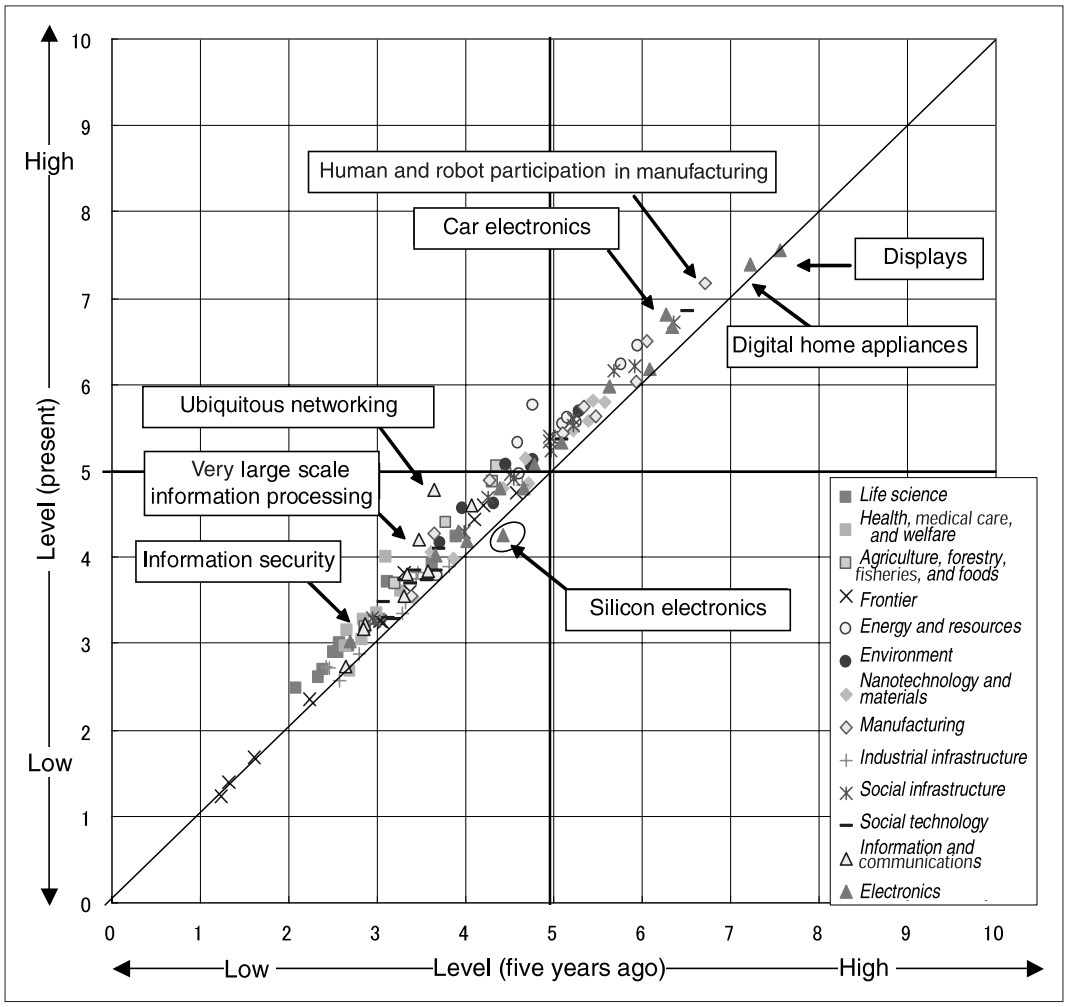
1 Introduction

The "Delphi analysis report [1]" on "The 8th Science and Technology Foresight Survey" published by the National Institute of Science and Technology Policy (NISTEP) shows Japan's R&D level. R&D comparisons are made with the U.S. for the past five years and are shown in Figure 1. Though most areas show progress, the area of silicon electronics indicates a loss of competitiveness. Assessing the increase in intellectual property, effect on the economy and the effect on society, the Delphi report

Figure 1 : R&D level of Japan in comparison with the U.S.: present and five years ago



Source: 'The 8th Science and Technology Foresight Survey'

emphasizes the importance of silicon electronics. In spite of this importance, Japan is reportedly losing its competitive edge in silicon electronics.

At present, silicon electronics faces a variety of challenges that include a requirement for highly sophisticated design technology to build complicated systems and physical limitations that limit further miniaturization of elements and interconnections. This article focuses on the interconnection issue, which is directly related to the development of high-speed LSI chips. Considering a silicon CMOS logic LSI chip, the interconnection issue is analyzed, showing the present status and challenges in design and manufacturing technology in conjunction with the interconnection issue. Finally, some proposals are presented to address these issues.

2 Interconnection issue

In LSI chips, a logic gate (AND, NAND, etc.) is formed by combining circuit elements (transistor, resistor, etc.) and the logic gate forms a macro for a sophisticated logic function. Interconnections connect the circuit elements, the gate, and the macro (hereinafter called "circuit components"), to each other. Interconnection of signal lines is mainly discussed in this article, due to its crucial role in LSI chip performance. However, the interconnection also includes power and ground lines in the general meaning. As miniaturization proceeds, the interconnection issue has begun to limit the performance and the manufacturability of LSI chips, where interconnection must be optimized through design and manufacture.

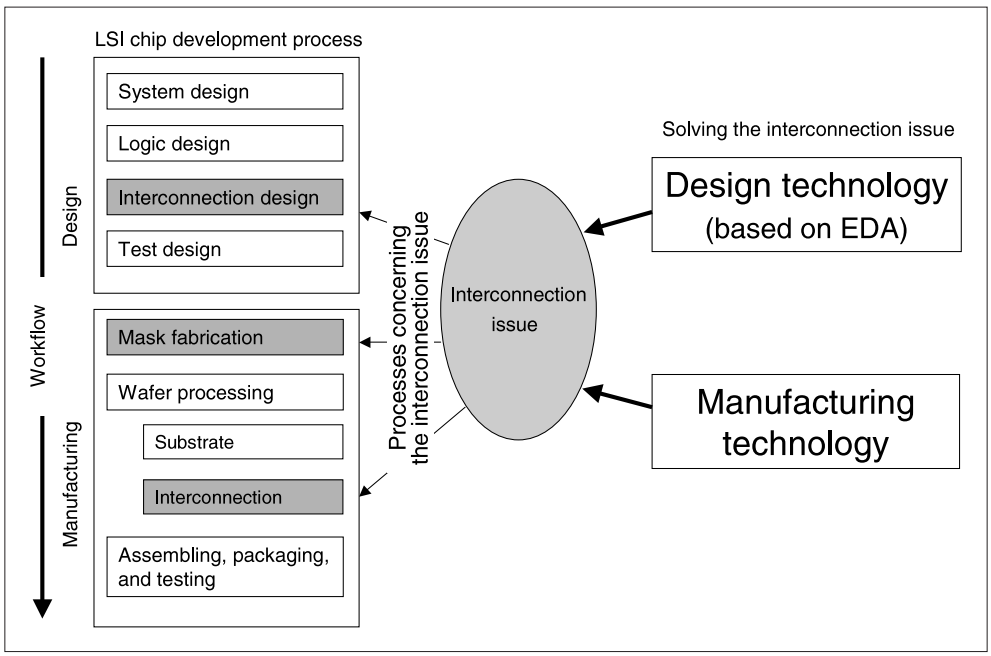
The interconnection issue is positioned in the LSI chip development process as shown in Figure 2. The process is divided between design and manufacturing. The interconnection issue appears several times, in the interconnection design [*1] when designing, in the mask fabrication process and in the interconnection process when manufacturing.

The interconnection design prepares mask data, optimizing placement and interconnection of circuit components. The mask fabrication process provides a mask based on the mask data, considering the lithography[*2] process. The interconnection process achieves the physical connections on an actual wafer. The interconnection issue is solved by the balanced use of design technology[*3] (also known as the design methodology) based on electronic design automation (EDA), and manufacturing technology realizing physical interconnections combining materials, architecture and interconnection technology.

2-1 Interconnection architecture

The multi-layered interconnection in an

Figure 2 : LSI chip development process and the "interconnection issue"



Source: Prepared by the STFC

LSI chip is shown schematically in Figure 3. Starting at the bottom, an LSI chip consists of, a silicon substrate where transistors and resistors are constructed, and an interconnection layer that provides connections between circuit components.

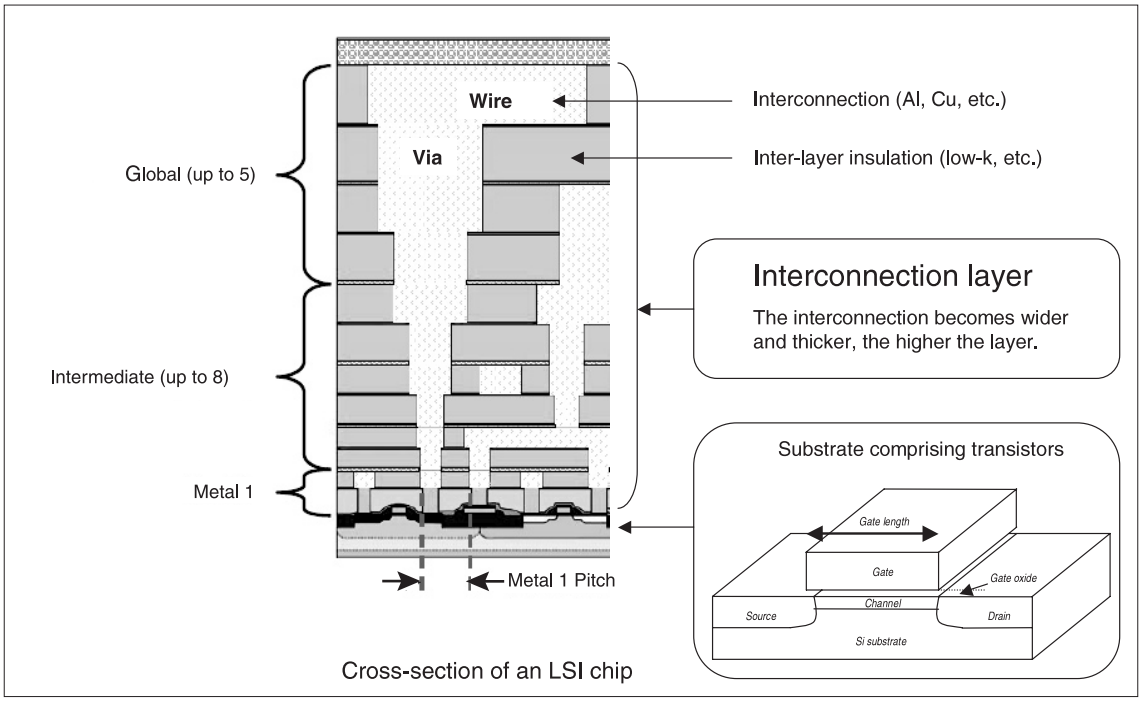
The interconnection layer is comprised of a series of vertical and horizontal interconnection lines, which form a connection overpass or underpass. The three-dimensional layered architecture of the vertical and the horizontal layer is called the multi-layered interconnection. The multi-layered interconnection is classified for each function and includes; a metal1 layer containing short interconnections between transistors and resistors; a global layer containing a clock signal line that covers the whole LSI chip; a power and ground layer (the uppermost layer) containing the power-supply and ground; and an Intermediate layer containing other functions. Miniaturization increases the numbers of interconnections inside an LSI chip to a few tens of millions of lines, increases the number of layers, and a rate of interconnection process within manufacturing process.

2-2 Signal propagation delay time

When a signal passes along the line, signal-propagation delay occurs. Every line has a resistance (line resistance) and capacitance (line capacitance). Here, the line capacitance includes the parasitic capacitance between neighboring lines. Proportional to the product of the capacitance and the resistance, the propagation delay increases as the line becomes longer due to higher capacitance and resistance. Though miniaturization should theoretically reduce the propagation delay, in reality it increases, because of the increases in coupling capacitance between narrower lines and the increase of resistance that results from having narrower lines. The signal delay is affected by miniaturization, as shown in Figure 4.

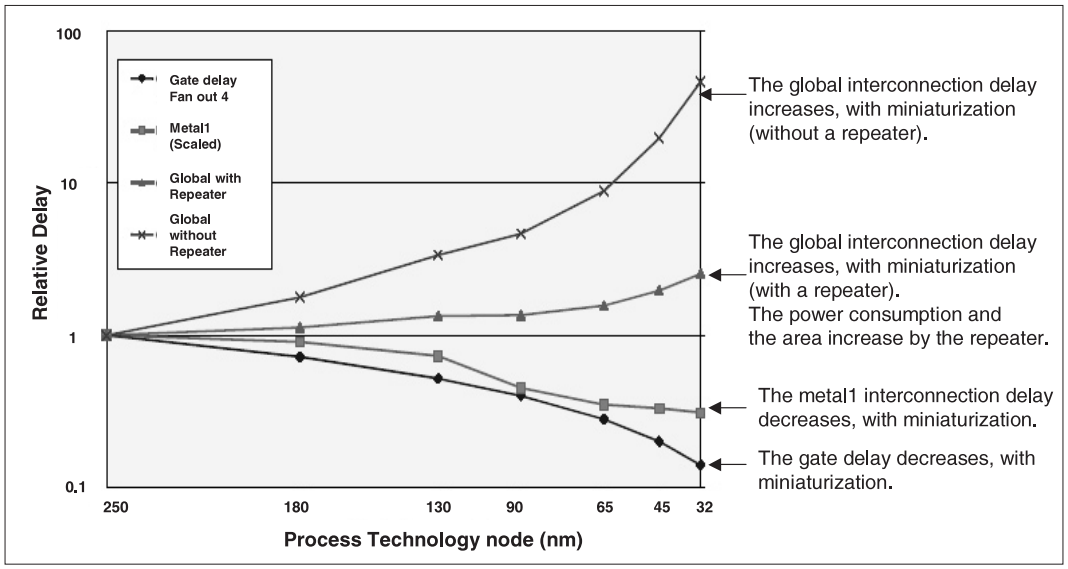
In Figure 4, the ratios of the relative signal and gate delay are shown, in which Cu is used as a conductor and a low permittivity (low-k) material as an insulator. Miniaturization reduces the gate delay and the line delay in the metal1 layer, while increasing the signal delay of the global interconnection. If a repeater (a buffer circuit to increase drive power) is inserted to reduce the signal delay, power consumption and area increase. The interconnection delay therefore affects the LSI chip's processing speed more than the gate delay does, when the technology node (node: half of the minimum line pitch) is less than

Figure 3 : Multi-layered interconnection inside an LSI chip



Source: Prepared by the STFC from ITRS 2003 report [2]

Figure 4 : Signal delay accompanied by miniaturization



Source: Prepared by the STFC from ITRS 2003 report [2]

250 nm. Minimized signal-line delay is necessary to achieve faster processing [3].

2-3 *Clock distribution and skew*

Clock distribution and skew are critically influenced by the signal delay when higher clock frequencies are employed. Synchronous circuits are dominant in existing LSI chip designs and in these circuits a clock signal must be simultaneously provided to tens or hundreds of thousands of flip-flops *4 in the LSI chip. This is called the clock distribution. The clock signal causes delay and leads to clock skew (a variation in the arrival time of all the clock signals). The clock skew limits the maximum clock frequency and causes malfunctions when the skew exceeds a critical limit. As clock frequencies become higher, the clock skew becomes more and more crucial to achieving faster processing.

2-4 *Additional issues related to interconnection[4]*

(1) Cross-talk noise

A smaller line pitch increases the capacitance between neighboring lines and causes signal leakage between lines (cross-talk). Caused by the voltage change of neighboring lines, the capacitance varies, changing the delay time (this is sometimes included in the cross-talk). Cross-talk deteriorates the signal integrity (quality of the signal shape), causing malfunction of the circuits. Therefore, cross-talk must be properly suppressed.

(2) Power consumption at interconnection lines

Historically, the gate consumed the largest amount of a chip's power but today Joule heat (heat generated by current through a resistor) consumes most of the power in CMOS devices. It is caused by the charge/discharge current of interconnection capacitance. In particular, a clock line forms a huge number of long interconnections that switch on/off at every clock signal, consuming more electric power than before. Less power-consumption at a signal line is a critical problem to be solved.

(3) Electro-migration

Electro-migration refers to the migration of an atom bombarded by an electron when high-density current flows, leading to a breakdown of a line. Miniaturization reduces the cross-section of a line, while a high clock-frequency increases the operating current. Therefore the current density is increasing, which increases the possibility of electro-migration.

3 R&D on the interconnection manufacturing technology

The interconnection manufacturing technology is related to a manufacturing process, its equipment, and the manufacturing line. In this chapter, the interconnection materials and architecture, and related research, is discussed.

3-1 R&D on materials and architecture

A number of studies (including research on materials and architecture) are underway regarding interconnection processes (interconnection-layer fabrication, insulation-layer, and inter-layer connection). In fact, at the moment, studies are mainly concentrating on[3]; material replacement from high resistance to low (Cu), low-permittivity (low-k) material development in order to reduce capacitance between lines, and via hole formation (constructing vertical metal connections between horizontal interconnection layers).

3-2 Interconnection technology under R&D

In the field of interconnection technology, research on reducing the connection length is underway. New types of connection, using light or electromagnetic waves, have been proposed for high speed transmission.

(1) On-chip transmission line

A transmission line transmits a signal at the speed of an electromagnetic wave, combining high-speed signal transmission with low power consumption. A differential transmission line, which transmits a signal using the voltage difference between two signal lines, cancels external noise and reduces the amplitude of the signal. Capable of high-speed transmission, the on-chip transmission line does not reduce the area of the line. Employed for a clock line or a long-distance interconnection, the transmission line will be able to accommodate a higher frequency of processing[5, 6].

(2) Three-dimensional stack architecture

The three-dimensional stack architecture allows multiple LSI chips to be stacked and connected to each other. So far, both wired and wireless interconnection methods have been studied. Using only vertical interconnection lines, the architecture reduces the propagation delay time when compared to conventional methods (interconnecting LSI chips through pads located on the peripheral area of each LSI chip).

The wired architecture stacks a number of LSI chips on top of one another and connects them using chip-buried interconnection lines. The chip-buried line carries a signal between the chips. Pioneering applications of this three-dimensional stack architecture that have already been constructed include an artificial retina chip and a vision chip [7].

The wireless method communicates between chips using inductance coupling or via an electromagnetic wave. With inductance coupling, the LSI chips communicate with each other by a magnetic field, using a pair of inductors fabricated on LSI chips [8-10]. With an electromagnetic wave, the high-frequency wave propagates between LSI chips using transmitting/receiving micro-antennas. This architecture allows data transmission among multiple LSI chips, and is used for simultaneous clock- or data-signal transmission [8].

Incorporating multiple inter-LSI chip interconnections, the three-dimensional stack architecture has the advantage of making parallel data transmission possible. This enables the high-speed communication between a CPU and a memory chip that is necessary for high-performance computing. The present EDA tools design only the two-dimensional architecture, indicating a need for new tools for placement and routing, and analyzing the three-dimensional architecture of circuit components.

(3) On-chip optical interconnection

Promising elemental technologies (a silicon light guide, a photonic crystal, a polymer light guide, etc.) have been studied for applying to on-chip optical interconnection. An ultra-fast nano-photodiode (photodetector) has been demonstrated using silicon and there are plans to apply this technique to a photoelectric transducer[11], though a compound semiconductor has already been used in this field. A silicon laser transmitting a continuous wave has also been demonstrated, which suggests that a photodevice (where communication inside a computer is achieved at the speed of light) could possibly be made commercially available at low cost [12].

The on-chip optical interconnection has advantages that include no interference at interconnection crossings, no cross-talk between high-density signal lines and is expected to be

used for clock distribution in order to achieve high-speed processing.

(4) R&D organization and formation

In the U.S., a collaborative R&D company, Microelectronics Advanced Research Corporation (MARCO), has funded university research and is conducting an R&D program called the Focus Center Research Program (FCRP). The Interconnect Focus Center (IFC) is included in the program and is conducting advanced studies on electric and optical interconnection[13]. A consortium of private companies, SEMATECH, is planning research on three-dimensional interconnections [14].

On October 13, 2005, the New Energy and Industrial Technology Development Organization (NEDO) in Japan advertised a preliminary survey on the industry-university-government collaboration program planned by the Millennium Research for Advanced Information Technology (MIRAI) [15, 16]. The program is researching "frontier interconnection development" and is planning to develop new interconnection technology for a post-45nm-node integration circuit. It is looking at ultra-low resistance interconnections, a new concept of global interconnection. The program will investigate ultra-low resistance interconnections using new materials (carbon nanotubes (CNT), etc.), photo-interconnection, and radio-frequency (RF) interconnection.

4 R&D on interconnection design

Design technology is comprised of designing architecture, a circuit, and the supporting tools. In this chapter, we will focus on the LSI chip design technology that is supported by EDA tools. Design technology is a methodology to design an optimized LSI chip, and is established by a design environment that details the design flow using EDA tools, libraries, and design equipment. There are several design phases such as system design, logic design, interconnection design, test design, and circuit design for circuit components, etc. Among them, here, closely related to the interconnection issue, interconnection design is described.

The interconnection design realizes a placement of circuit components and incorporates interconnection lines correctly within a limited size of LSI. At the same time, it needs timing design for the desired performance and finally, checks the whole design. The present trend of research into interconnection design is presented in the following sections.

(1) Design rule

The design rule governs the whole LSI design process, based on available materials, architecture, and interconnection technology. Sizes of circuit components, spacing between neighboring components, three-dimensional layout of components, etc., are all defined by the design rule. It is necessary to build miniaturized circuit components and interconnection lines, and to be able to manufacture on a mass production scale. In addition to the above rule, a design flow uses a number of design parameters (resistance and capacitance of an interconnection line, interconnection capacitance and cross-talk between neighboring lines, etc.) to obtain a correct result. These parameters are also incorporated into the design rule. The design rule is an interface to designing interconnection that considers manufacturing limitations and should be followed rigorously to obtain a good quality design.

(2) Timing issue challenges

Mistiming leads to malfunction of the LSI chip, even when it consists of flawless logic circuits. Timing design draws most attention among the present LSI chip design processes and must make allowances for signal delay. The signal delay is governed by the clock distribution and must be less than the allowable delay limit of signal propagation. The allowable delay limit is defined by the longest or shortest propagation time between flip-flops or between a flip-flop and an external terminal. The delay of all signals must be within the limits.

The timing issue is solved in a number of ways: using a distribution method of the clock signal, using automatic interconnection layout to minimize the clock skew, by the insertion of

buffer circuits or by optimization of the signal line width at the line that violates the delay limit, and by verifying the timing (discussed later).

A design method combined with timing design has been presented for a microprocessor [17], in which most of the design time is spent on timing design. This implies that the timing design is complicated and requires expertise.

(3) Design check

An automatic design tool that satisfies all the requirements of a design rule has not yet been developed. Combining placement and routing using automatic tools and manual interconnection designs, the design must be checked to ensure that it meets the requirements. Design rule check (DRC) has been widely used to check that the design meets the requirements and has resulted in communication between design and manufacture. Recently, DRC has been found to be insufficient for obtaining high manufacturing yields.

Attempts have been made to solve the timing issue by using tools that perform static timing verification (checking the delay limit in all logic paths) and statistical static timing verification (considering manufacturing variations of LSI chips). The cross-talk issue has been approached in the same way, with a tool to analyze cross-talk between lines inside an LSI chip and another to check timing in which cross-talk is converted to delay time. In addition, other tools (transmission line analysis, power consumption analysis, electromagnetic analysis, thermal analysis, etc.) are used, and are increasing in importance.

The checking tools complement the EDA tools. Based on the output of the checking tools, the design is revised by hand, which requires a long time and can deteriorate the design quality. Therefore, those functions are being incorporated into the EDA tool portfolios.

(4) R&D trend of EDA tools for interconnection design

In the 1980s, the tools for designing interconnections were intensively developed, providing a high quality of layout and interconnection design. In the 1990s, the focus shifted to a system design tool and a logic design tool. From the end of the 1990s, the high-integration of LSI chips again required the development of interconnection-design EDA tools. At the 42nd Design Automation Conference (DAC), in June 2005, presentations on interconnection design (physical/circuit design, timing and design for manufacturability (DFM)) accounted for about 35% (65 publications) of the total number of presentations.

5 Trend of design technology and related tasks

The interconnection issue is solved with the balanced progress of manufacturing technology and design technology, as described in Chapter 2. How competitive are these technologies in Japan?

Japan has a history of leading the world in the manufacturing technology market, although it seems to have lost some market share recently. Japan lost the majority share of DRAM production to South Korea, has been slow in the standardization of microprocessors, and has lost some share to the foundry businesses in Taiwan. The manufacturing technology industry in Japan is still at a high level, particularly in the area that vertically integrates design and manufacturing. An advanced study for interconnection has been conducted in universities and companies in Japan and is held in high regard by the global community.

In contrast, the design technology market is dominated by the U.S., which incorporates design know-how into EDA tools. From the viewpoint of balanced progress, the design technology in Japan (heavily dependent on U.S. EDA tools now) must be developed in order to solve the interconnection issue. Realizing that present advanced technology must be accompanied by the integration of design and manufacture, it is essential that design technology be developed. The present trends and challenges of design technology are discussed in this chapter.

5-1 Design technology trends

Figure 5 shows the position of the interconnection design in LSI development and the progress of that development for further miniaturization. Though the development

comprises design and manufacturing, at the time when designing is closely linked to manufacturing, the design process is not clearly separated from manufacturing. This is due to an increasing dependency on the physical properties of an LSI chip, resulting in further complication of the design process. So far, cooperative specialization has been fostered in this industry: a design division (designing and transferring the design in the form of master data to a manufacturing division), a manufacturing division (manufacturing of LSI chips using a photo-mask), and a design division (checking the product). The border among divisions is becoming blurred, as shown in Figure 5.

(1) Independent logic and interconnection design (① in Figure 5)

In the past, an engineer in a design division designed interconnections after checking the logic design. The logic and interconnection design processes were iterative when the design was modified. Though both processes were, therefore, not completely separate, they were mostly independent of each other.

(2) Integrated logic and interconnection design (② in Figure 5)

When miniaturization induced an interconnection delay that was more dominant than the gate delay, conventional design (simple interconnection of the circuit components) became incapable of meeting the delay-time limit. Therefore, the logic design was modified after the interconnection design was completed. Calculating the delay time and a critical path in the logic path of signal propagation, the logic and the interconnection designs were matched by modifying the drive capability of a gate on the critical path, for instance. This design method is known as integrated logic and interconnection design (see Figure 5).

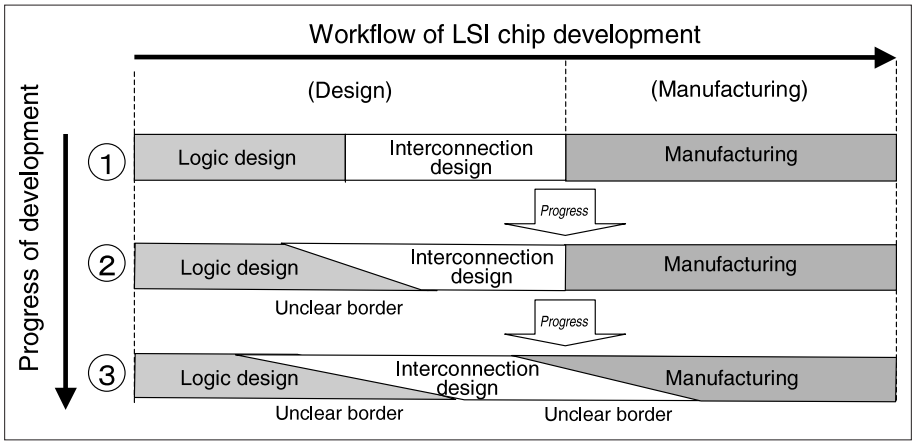
(3) Integrated design and manufacturing (③ in Figure 5)

Further progress in miniaturization caused a new problem in manufacturing - that of the size limit of lithography. The width of the interconnection line became smaller than the wavelength of light in lithography, which greatly impacted manufacturing yield. This was caused by the breakdown of a line and short between lines due to the deformation of mask data in manufacturing process. Some ways to correct a mask during manufacturing became unfeasible. Therefore, the integration of design and manufacturing was introduced, in which interconnection design was carried out in order to increase the manufacturing yield.

5-2 Blurred border between design and manufacturing

Integrated design and manufacturing is typically observed in a phase-shift (PS) mask[*5] and an optical proximity correction (OPC) mask[*6] [18], where the mask is modified in order to increase pattern resolution at lithography. Advanced manufacturing technology that

Figure 5 : Progress of LSI chip development with advancing miniaturization



Note: the system design and the test design are not included for clarity.

Source: Prepared by the STFC

integrates design technology is of increasing necessity for achieving better yield when manufacturing governs line width and limits the number of via holes.

Dr. Shimohigashi, Semiconductor Technology Academic Research Center, emphasizes the importance of the beyond-the-border design and manufacturing, addressing [19], "The coming nanometer scale CMOS chip faces a number of problems, one of which is design for manufacturability (DFM). The DFM is defined as an action spanning all design processes in order to maximize the product manufacturability. The DFM at the nanometer level is particularly characterized by its scale and complexity. Miniaturization has been accompanied by side effects that threaten to limit further miniaturization. A new workflow is necessary, in which design and manufacturing work harmoniously and systematically."

5-3 Increase of design challenges

Miniaturization increases design challenges, as shown in Figure 6. A new issue becomes evident; the issue revealed becomes complicated as miniaturization proceeds, and the complexity increases exponentially.

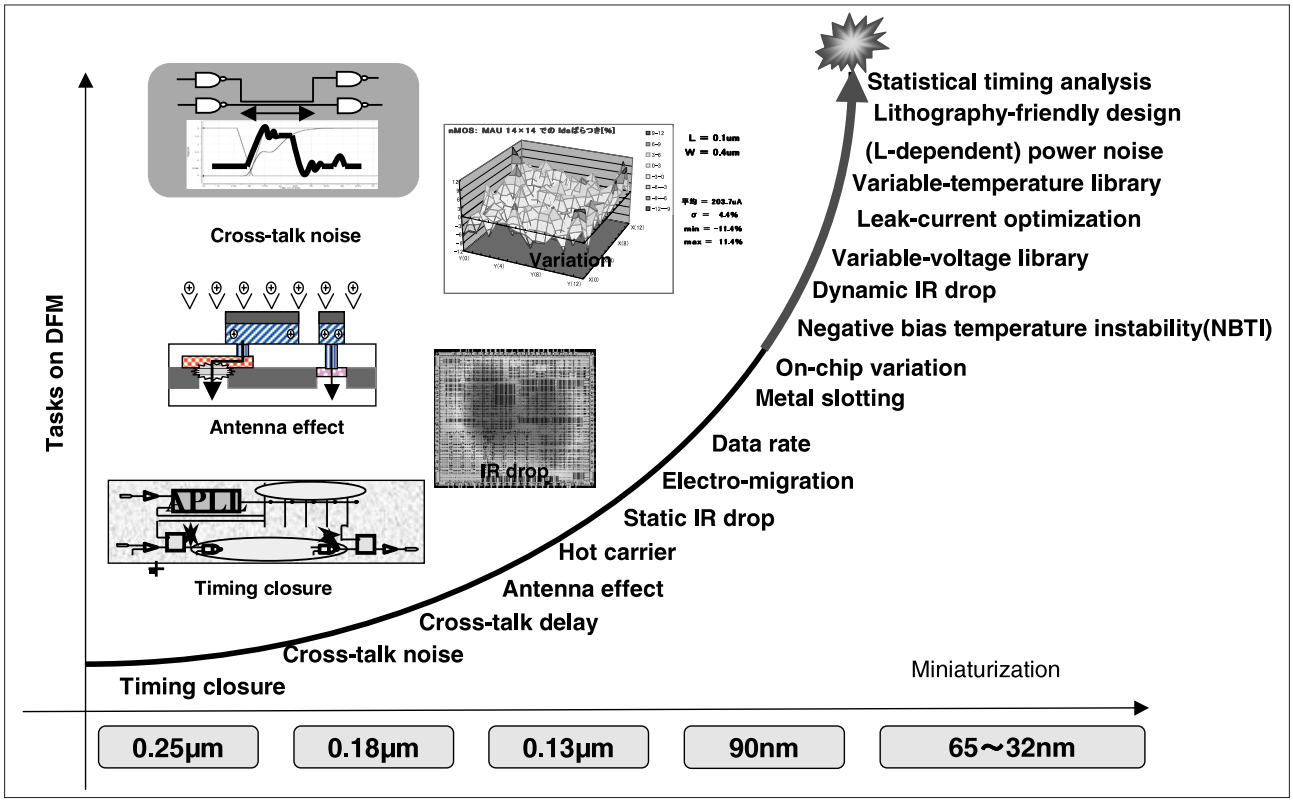
A CPU chip incorporates 60 million transistors, a few hundred meters of interconnection lines, and nearly a billion via holes for connecting lines. Reportedly, the more connections there are, the worse the LSI manufacturing yield is. The yield therefore seems to be governed not by the number of transistors, but by the number of interconnection lines.

5-4 Design-conscious manufacturing technology

The number of presentations related to multi-layered interconnection technology at the IEEE's International Interconnect Technology Conference (IITC), a major conference in the field of interconnection, are summarized by region in Figure 7. In the U.S. and Europe, R&D is under way and is multilaterally approaching the multi-layered interconnection technology, focusing on design technology. In contrast, the multilateral approach is rare in Japan.

Manufacturing technology is developed when a higher-level requirement must be met, at which point it becomes more closely integrated with design technology. It is necessary to develop

Figure 6 : Increasing design tasks with the progress of miniaturization



Source: Provided by the Semiconductor Technology Academic Research Center (STARC)

manufacturing technology when the boundary between designing and manufacturing becomes unclear.

5-5 Dominance of U.S. commercial EDA tools

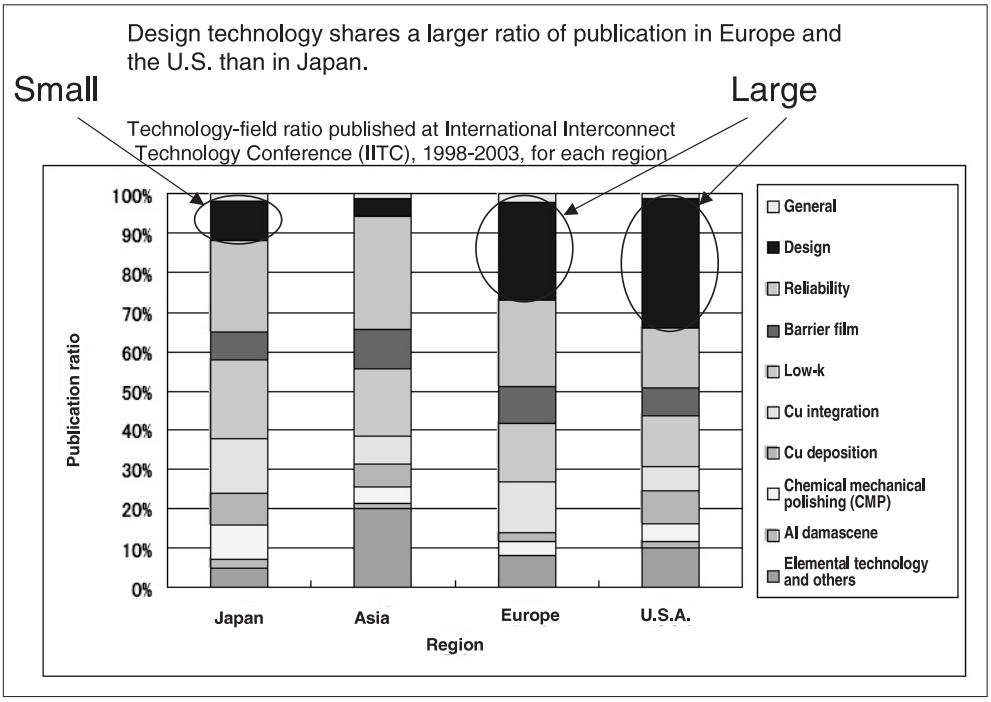
Most commercially available EDA tools are, at present, developed by EDA vendors in the U.S.

The present status of EDA tools in Japan has been described as follows [20]; "In the 1990s, many Japanese companies stopped developing EDA technology in house and LSI chips were primarily designed using EDA tools provided by vendors in the U.S. and Europe. The commercially available tools are more cost effective than in-house development, in the short-term. Giving up in-house development may have a huge impact when considering long-term strategies... EDA tools cannot be used effectively without understanding how they are designed and developed. This is because the tool evolves due to knowledge accumulated through LSI chip designs. R&D on EDA tools definitely improves the quality of designing." Design technology progresses in the course of iterative design and problem solving. The EDA tools for interconnection are, however, developed by a limited number of companies in Japan, due to the huge cost of development as the EDA system becomes gigantic in size. In parallel with giving up development in companies, researchers in universities have moved to other research areas. The present status is the result of the trend previously described here. Excess dependency on commercially available foreign EDA tools may deprive Japan of a competitive edge in the technology.

Even though depending on commercial available EDA tools, it is not easy to utilize them. The EDA tools must be matched to a specific task and are properly chosen to represent the design culture. A suitable EDA tool is chosen by an experienced and developed engineer, who can check the tool in a variety of ways: experience of designing and using the tools, understanding of benchmark testing, and experience in LSI chip development and manufacturing. Experienced engineers who developed the tools are now in charge of tool choice and passing on that expertise. However, the number of experienced engineers available to pass on that expertise is also declining.

In the era of increasingly complex LSI chips, Japan finds itself in a crisis situation.

Figure7 : Publication ratio on multi-layered interconnection technology combined with design technology (for each region)



Prepared by the STFC from Japan Patent Office report [3]

5-6 Protection of secrets

An equipment-recipe patent is commonly used for protecting manufacturing intellectual property, which works efficiently to protect manufacturing secrets as a patented product, instead of a patented manufacturing method. The equipment-recipe patent is defined as "a software patent for a method of controlling manufacturing, in the form of software, a memory medium, or recording media." At present, foundry companies are considering protecting their software equipment control methods using equipment-recipe patents. Semiconductor manufacturers in Japan are now wondering if they have disclosed too much information about how they use the equipment to equipment manufacturers, without legally protecting that knowledge [3].

The same type of disclosure without protection may have also occurred in the use of EDA tools. The users of EDA tools in Japan (semiconductor or computer manufacturers) are now wondering if they too have disclosed too much information about how they use the tools to EDA vendors, without legally protecting that knowledge. The users are wondering if they have been providing their valuable expertise for free.

EDA tools require a variety of expertise in designing. An EDA tool is not perfectly built, and this is compensated for by the knowledge of its users. EDA tools are refined and become more competitive in the world market by incorporating demands for correcting any problems or adding extra functions. In this way, design know-how is unintentionally leaked to vendors.

Most secrets in manufacturing are confidential information, which should be legally protected at the time of integrating design and manufacturing.

6 Future actions and related proposals

The balanced development of design and manufacturing technology is necessary for solving the interconnection issue, as described previously. Miniaturization is now forcing big changes to the design process: that of timing adjustment meeting the delay limits and the integration of design and manufacturing. Both are caused by the interconnection issue. The technology is now at the stage of systematic integration of the whole system. The integration is a worldwide task, and is a critical issue in specialized manufacturing (fabless or foundry business). Though EDA tools show rapid progress, progress cannot keep up with the rapidly evolving complexity of LSI chips. This might be a chance to build design technology linked to manufacturing technology, an industry in which Japan has an advantage. The promotion of the design technology for solving the interconnection issue is proposed as follows.

6-1 Promotion of the design technology: development of core EDA tools (industry-university-government collaboration from a long-term perspective)

The industry in Japan has an advantage in timing adjustment knowledge and in the integration of design and manufacturing. The domestically developed core EDA tools provide competitiveness in the EDA tool market and in the LSI chips designed using the tools. EDA tools for 'analog RF hybrid design,' which is used for designing products in competitive industries in Japan (digital information home appliances, cars, robots, etc.), have not been well developed yet, even in the U.S. Early development of the tools will also be advantageous to the related LSI chips. Throughout the development of these tools, design expertise and technology should be accumulated, passed on, and protected. The way to promote the development is presented in detail below.

(1) Development of an advanced design method and EDA tools that maximize the advantage of manufacturing technology

A design rule must be defined prior to the development of the design method, when the design technology is developed by integrating manufacturing technology for advanced products. Comprising both design and manufacturing, the design rule must be defined without forcing a bias to one side or the other. This requires a quantitative evaluation to assess the investment effect brought about by employing the rule. The evaluation assesses how the

interconnection rule affects the manufacturing yield and the timing issue. If the evaluation is not sufficient, the integration does not work well. Domestically developed EDA tools incorporate the specifications required for EDA tools, which optimizes the design workflow that the design technology provides. Discussing the R&D trends of the interconnection technology in Chapter 3, a new design method and EDA tools should be forthcoming and developed with the future in mind. Targeting R&D on EDA tools for the product segment in which Japanese companies have superiority, is a promising and effective approach.

Together with EDA tools for the interconnection issue, EDA tools for system, logic and test design should be enhanced in order to improve quality and the productivity of the design.

(2) Interdisciplinary Collaboration

Development of the EDA design tool requires knowledge of both design and manufacturing and a deep understanding of physics, as the miniaturization is approaching the physical limit of size. A specialized workforce cannot independently develop the tools, and collaboration with other specialties must be considered. Collaboration and information sharing among researchers and design/manufacturing engineers, including engineers at equipment manufacturers, are also desirable. EDA tools are useful and competitive when they incorporate input on solving issues presented by equipment manufacturers.

Collaboration between scientists working in silicon technology and nanotechnology is to be highly encouraged. Computation science on analysis of high or low permittivity material has shown potential [21, 22], and technology computer aided design (TCAD) has shown potential as the basis of process development, even though these fields are not specifically related to interconnection design. Miniaturization has reached the nanometer scale and while many technology fields can no longer work in isolation, interdisciplinary study may revolutionize the LSI chip development environment. Therefore, cross-field collaboration should be actively promoted.

(3) Organization and management to promote development

The interconnection issue is solved only when the issue represents a real and critical problem at design and manufacturing in a company. The establishment of a consortium made up of private companies is therefore inevitable. Researchers in universities are encouraged to join and contribute to these consortiums, providing scientific and theoretical knowledge. A committee of the consortium must carefully handle the results developed by the consortium. Some are not disclosed outside the consortium participants and some are proposed to be made available to the whole industry to achieve standardization.

Motivation among researchers in universities is one of the issues when promoting collaboration among companies and universities. Some research is kept confidential, and it cannot be used for publications which sometimes assess job performance. This might be addressed by changing the assessment method used to evaluate job performance. Funds provided by industry/university collaboration could be assessed in the same way as publication and patents, for example. Despite this difficulty, many researchers in universities outside Japan have been achieving impressive results in their design research. The assessment issue may be solved in Japan as well.

6-2 Balanced cutting-edge between manufacturing and designing technology

(1) Active promotion of intellectual property (short-term proposal to industry)

Integration between design and manufacturing has several options depending on where in a design workflow a solver for defect issues is positioned. For example, logic design, or interconnection design, where the defect issues include a defect caused by dust, a process defect, a lithography defect, or a random defect. The options or a combination of options is valuable as intellectual property, directly in conjunction with the manufacturing yield. The intellectual property must be clearly classified as a patent or as confidential information. Intellectual property is classified by how easy a violation is to find. So,

if a violation is easily found it is classified as a patent (for example, an interconnection pattern), and if a violation is not easily found it is classified as confidential information (for example, information or an analysis method to enhance a manufacturing yield).

The confidential information should be protected from free access by unauthorized employees, using a fully equipped security system.

Design secrets are not protected only by the domestically developed EDA tools (see 6-1). The LSI chip design flow is carried out by combining commercially available EDA tools and domestically developed (or in-house developed) tools (called core tools or solvers). When commercially available EDA tools are used, secrets are considered very valuable and should be protected. Parameters and expertise for using commercially available EDA tools are proposed to be translated to some manageable products, such as software used for an equipment-recipe patent. Adopting a graphical user-interface should be considered because it works well when lodging claims for intellectual property violations.

(2) Clarified targets (mid- or long-term promotion by the government)

By incorporating advanced R&D, technology can be revolutionized. The orientation of each research area must be highly aligned, and requires a clearly defined target. The government should take responsibility for clarifying this target, especially ones with great propagation effect. Based on the target, the government should promote R&D for each elemental technology, followed by commercialization by a company, which is the desired cycle of R&D and commercialization.

Research is now being conducted separately to achieve high-speed processing and low power consumption. Especially, the development of low-power-consumption LSI chips for information home appliances is emphasized. In principle, however, high speed and the low power consumption are inseparable. R&D should be encouraged to achieve high-speed processing, as well as low power consumption. LSI chips for cellular phones are, for example, being developed to achieve high-speed processing, as these phones have more and more functions that require this level of processing power. LSI chips for cars are being developed in order to achieve high tolerance under severe conditions, as LSI chip used in cars is rapidly expanding [23]. The roadmap presented by NEDO is focused on low-power consumption technology [24], while a roadmap focusing on high-performance technology is expected as well.

One candidate for high-speed processing is in the development of a CPU for a supercomputer, which aligns the direction of design and manufacturing technology in the pre-competitive field. In the past, advanced technology developed for a supercomputer was transferred to commercial systems and CMOS LSI chips, and is still being used in EDA tools that are trying to solve the interconnection issue caused by miniaturization.

Another candidate is the development of design and manufacturing technology that targets analog RF hybrid design, which aligns another direction of development. For high performance while still remaining within a strict power consumption limit, extremely advanced technology is required.

7 Conclusion

In this article, the interconnection issue in silicon electronics has been discussed, and R&D targets for this issue have been clarified. Policies to strengthen design technology to create the coming interconnection technology have also been proposed. This may play an important role in revitalizing silicon electronics in Japan. Accumulating design and manufacturing secrets, it is essential that EDA tools are developed for a competitive LSI chip industry, and this is one of the key R&D targets.

Acknowledgments

The author appreciates the information, advice, and materials provided by Prof. Atsushi Iwata (Executive Director, Research Center for Nanodevices and Systems, Hiroshima University), Prof. Kazuya Masu (Integrated Research Institute, Tokyo Institute of Technology), Visiting Prof. Yoichi Oshima (Precision and Intelligence

Laboratory, Tokyo Institute of Technology), Prof. Hidetoshi Onodera (Department of Communications and Computer Engineering, Graduate School of Informatics, Kyoto University), Prof. Shuji Tsukiyama (Department of Electrical, Electronic, and Communication Engineering, Faculty of Science and Engineering, Chuo University), Dr. Katsuhiro Shimohigashi (President and CEO, Semiconductor Technology Academic Research Center (STARC)), Dr. Masaki Hirata (Chief Researcher, Research & Development Department, STARC), Dr. Satoshi Ito (Chief Research Scientist, Advanced Functional Materials Laboratory, Corporate Research & Development Center, Toshiba Corp.), Dr. Koichi Kato (Chief Research Scientist, Advanced LSI Technology Laboratory, Corporate Research & Development Center, Toshiba Corp.), Mr. Masaru Katagiri (LSI Technology Expert, Computers Division, NEC Corp.), and Dr. Yasushi Igarashi (Project Coordinator, Electronic & Information Technology Development Department, NEDO).

Glossary

*1 Interconnection design
In this article, interconnection design carries a wider meaning: the whole design workflow related to physical design (placement of circuit components, interconnection among them, signal-timing test, electric test, design rule check, mask-data generation, etc.). Interconnection design is also called "physical design" or "layout design." In other papers, interconnection design, however, has a narrower meaning: designing an interconnection pattern among circuit components.

*2 Lithography
Lithography stands for all the equipment and processes used to develop a circuit pattern.

*3 Design technology
Design technology refers to the technology used to design an LSI chip, and comprises design technology for the architecture, circuits, etc., and other supporting design methods. In this article, "design technology" refers to the technology to design an LSI chip supported by EDA tools. With increasing integration and seeking high performance, "design technology" has become heavily dependent on EDA tools, and is closely linked to the progress of EDA tools.

*4 Flip-flop
A flip-flop is a memory circuit that has a high or low status. The status is held until the next signal arrives.

*5 Phase-shift (PS) mask
The phase-shift (PS) mask enhances the resolution of the pattern, using interference between phase-shifted and non-shifted light.

*6 Optical proximity correction (OPC) mask
The optical proximity correction (OPC) mask works by making small changes to the IC layout on the mask, reducing lithography distortion.

Abbreviations

•*CMOS*	Complementary Metal-oxide Semiconductor
•*DRAM*	Dynamic Random Access Memory
•*DRC*	Design Rule Check
•*EDA*	Electronic Design Automation
•*OPC*	Optical Proximity Correction
•*RF*	Radio Frequency
•*SEMATECH*	Semiconductor Manufacturing Technology Institute

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(Original Japanese version: published in December 2005)