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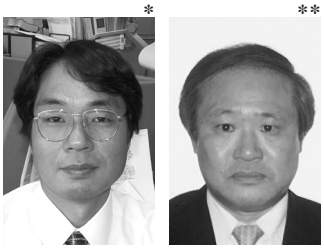
R&D Trends of LSI Design Technology
— Bottleneck at Development of System LSIs that rule Value-Added Electronic Devices —



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1 Introduction

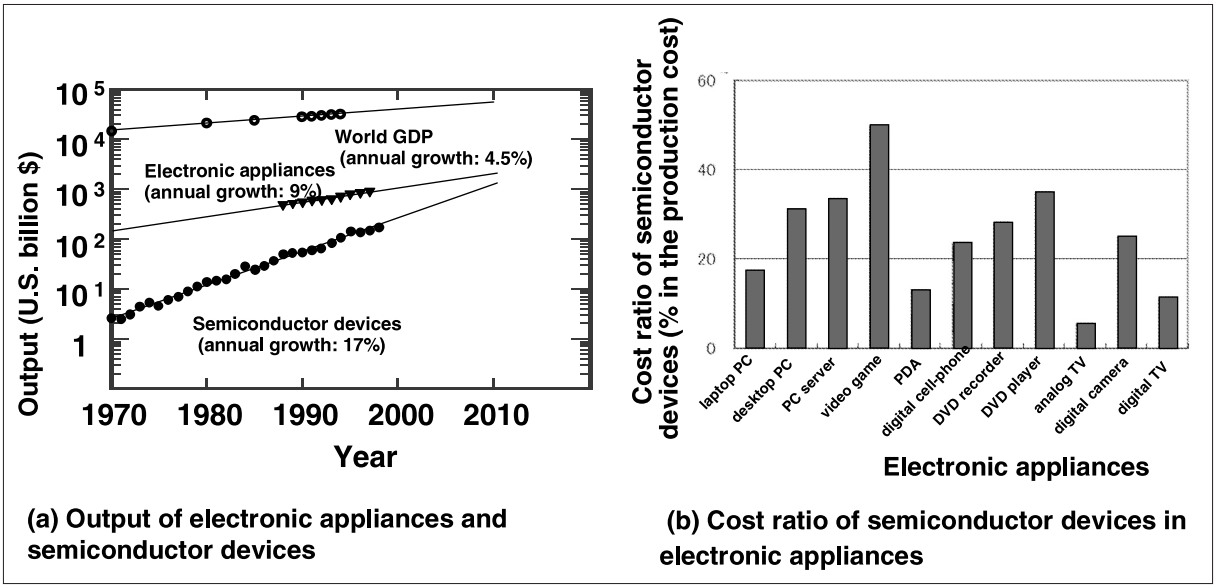
1-1 Much more value in an LSI

The progress of the semiconductor LSI technology has played a major role in the progress of advanced multi-functional electronic appliances, where such progress is represented by the LSI's increasing compactness, reduced power-consumption, and further multi-functionalities. Certain essential electronic components for appliances have been built using a couple of modules (a few centimeters in width and depth) capable of accommodating a few different kinds of LSIs. These modules are being replaced by system LSIs (a few millimeters in width and depth).

The system LSI critically affects the price and performance of the appliances. The annual output of electronic appliances and semiconductor devices is shown in Figure 1(a), together with the world GDP[1]. The GDP shows 4.5% of the mean annual growth rate, while the appliance output is shown as 9% of mean annual growth. This represents the fact that electronic appliances are increasingly consumed ahead of other purchases. The semiconductor device output shows 17% of mean annual growth, which is higher than that of appliances (9%), signifying that the importance of semiconductor devices is increasing among the components implemented in electronic appliances.

The cost ratios of semiconductor devices to the number of electronic appliances are shown in Figure 1(b)[2]. Digital technologies, when used alongside advanced signal processing, inevitably

Figure 1 : Annual output of electronic appliances and devices, and the cost ratio of semiconductors in appliances



(a) Output of electronic appliances and semiconductor devices

(b) Cost ratio of semiconductor devices in electronic appliances

Source: References[1, 2]

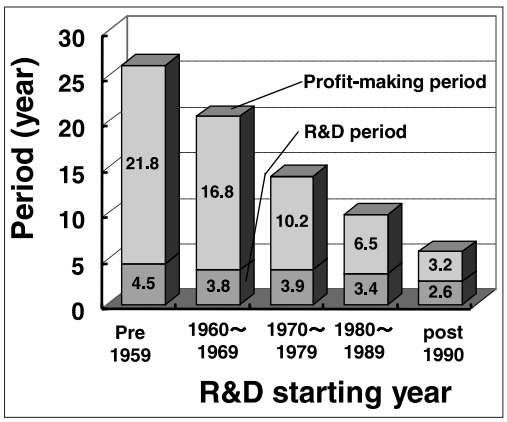
involve an increase in the semiconductor cost ratio. To be precise, this ratio sometimes reaches up to 50% in PCs and video game machines.

In future, the cost of electronic appliances will be governed by that of LSIs. The performance and cost of LSIs are essential for the successful business of electronic appliances, whereby the value of appliances is dominated by LSIs.

1-2 Encountering LSI design crisis

R&D and profit-making periods of products, services, and manufacturing (abbreviated as products hereafter) are plotted versus the R&D starting year in Figure 2. Over the last 30 to 40 years, the profit-making period has become ever-shorter compared with that of the R&D period. The ratio of both (profit-making/R&D) was about 5, but has since reverted to around 1.2, indicating a shortened product life-cycle.

Figure 2 : R&D periods and profit-making periods of products versus R&D starting years



Source: Prepared by the authors, based on reference[3]

Business success depends on technologies used to reduce the leading time (R&D period) in business circumstances involving shrinking product life-cycles. The technology for the swift development of LSIs is essential to the electronic appliance business.

However, system LSI development is facing a crisis. The productivity of silicon-semiconductor LSIs (in terms of the degree of integration) has been developed ahead of the roadmap (international technology roadmap for semiconductors (ITRS)), while the LSI design productivity has lagged behind that[4]. The number of transistors integrated in an LSI chip has increased by 58% annually (4 fold in 3 years), while the LSI design productivity per engineer has increased by as little as 21% a year, despite the introduction of design automation tools and increased computer power, as shown in Figure 3.

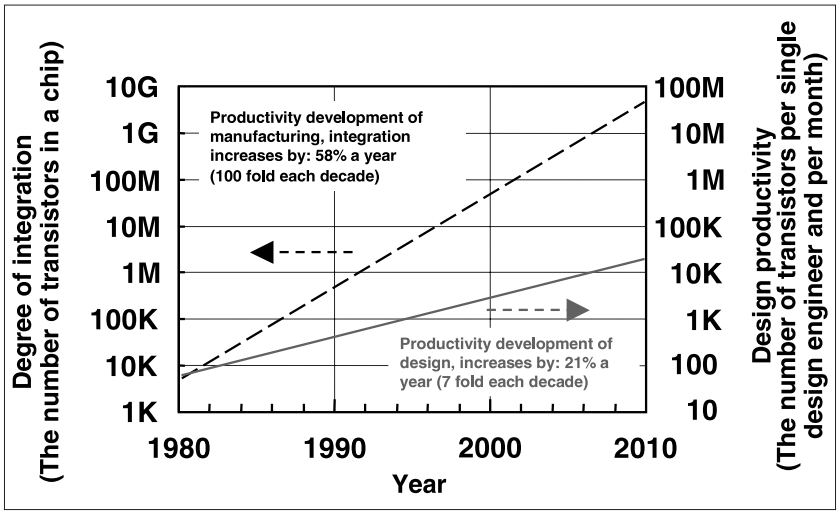
Focusing on system LSIs essential to electronic appliances' value, this feature article analyzes trends in LSI design technology and discusses present and future issues.

2 Design technology of LSIs

2-1 LSI design technology

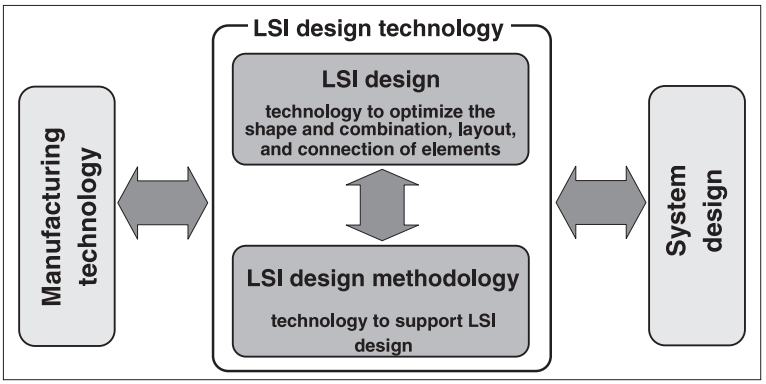
LSI design technology stands for technology used to design an LSI capable of logic operation and electronic properties that meet system requirements, optimizing the physical shape of elements, their combination, individual layout, and inter-element connection, on the basis of

Figure 3 : Maximum number of transistors in manufacturing and design



Source: ITRS

Figure 4 : LSI design technology



an available fabrication technology as shown in Figure 4.

During the optimization process, the technology can be subdivided into two (technology to design, and that to support the design), where the two technologies differ in nature and the knowledge required to use them. Their quality is evaluated using different characteristics, in many cases.

The quality of the design is, for example, evaluated by the chip performance design: processing speed, power consumption, etc. The quality of the support, meanwhile, is evaluated by the design productivity: the design period compared with the number of integrated elements, etc. When elements highly dependent on its manufacturing process are designed, the performance is optimized through a series of processes: initially, the modeling of physical phenomena and elemental characteristics; secondly, the model is replaced by a descriptive language; thirdly, elemental performance with regard to the element shape and size is computer-simulated; and finally, the performance is optimized without experimental fabrication. Accordingly, element design productivity is increased. Here, two processes play a particularly important role, namely: modeling, the means by which the description, representing the physical phenomena and element characteristics, is simplified without losing precision and reliability; and the period for designing, namely how quickly the performance is estimated with considerable precision and reliability.

Here, the technology with which LSIs are designed is called “LSI design,” while that used to support the LSI design is called “design methodology.” In this article, the latter, design methodology is discussed in detail.

2-2 Progress in design automation technology

Increasing the number of elements integrated in an LSI under Moore's law (exponential increase in the number of elements), LSIs have shown progress in design methodology to accompany the increase. The progress in electronic design automation (EDA) has been remarkable, as shown in Table 1.

The EDA technology has changed the style of description language every decade, while the number of elements in an LSI has increased 100 fold over the same period. The design methodology must have been changed drastically in order for design engineers to keep pace with the increase in elements, rather than minor improvement in the design process. The progress of the design methodology was achieved employing further abstract descriptive language, as shown in Figure 5. More upper notion, or more abstract language, has become essential with the increase in elements, owing to the limited number of logic circuits which can be simultaneously considered by design engineers.

In the course of the progress of EDA tools, a number of venture companies have been set up and selected, some of which have become well established firms providing a de facto standard for tools. However, the standards of some failed companies are still in use, such as the GDS II format (data format of a mask pattern, Calma Company, in the US).

Having developed as shown in Table 1 and Figure 5, the descriptive style of the LSI design is still based on “hierachical description level,” which was employed in the opening EDA phase.

2-3 Recent R&D trends

(1) Hardware/software co-design

After specifying the interface between hardware and software, each has been developed independently, in most cases. With an increase in system size, a variety of problems occurred, relating to ambiguity of the specification or certain other issues, shifting from hardware to software during the development process.

The hardware/software co-design is in contrast with the conventional design process, where the function and interface are defined to take account of the mutual trade-off, in the course of measuring and optimizing system performance, as shown in Figure 6(a), (c).

Sometimes, the priority of a certain function governs the choice of whether it is realized by mainly hardware or by mainly software. Here to realize LSI functions mainly by hardware means that special circuits are designed to satisfy each function of LSI. On the other hand to realize LSI functions mainly by software means that various software which works on general circuits is used to achieve LSI functions. Employing an increased number of application specific LSIs, the system achieves reduced power consumption and accelerated operation, which

Table 1 : Progress in LSI electronic design automation

Year	Description method	Description level	Remarks	Major tool vendors
'70 ~	Mask pattern	Physical shape of elements	Described using a two-dimensional layout pattern for each mask	Applicon (1969) Calma (1970) Computervision (1972)
'80 ~	Circuit diagram	Elements such as transistors	Described by element and logic gate symbols	Daisy (1980),Mentor (1981) SDA (1983, Reorganized to Cadence) Optimal Solutions Inc. (1986, Reorganized to Synopsis)
		Logic gate		
'90 ~	Text language	Register transfer	Described using text language to show data flow and a series of data processing	Syntest (1990)
		Transaction		
		Behavior	Each part of system behavior is described	CoWare (1996) TenSilica (1997)

Established years are in parentheses

Figure 5 : Progress in the descriptive style of LSI design and present hierarchical description level

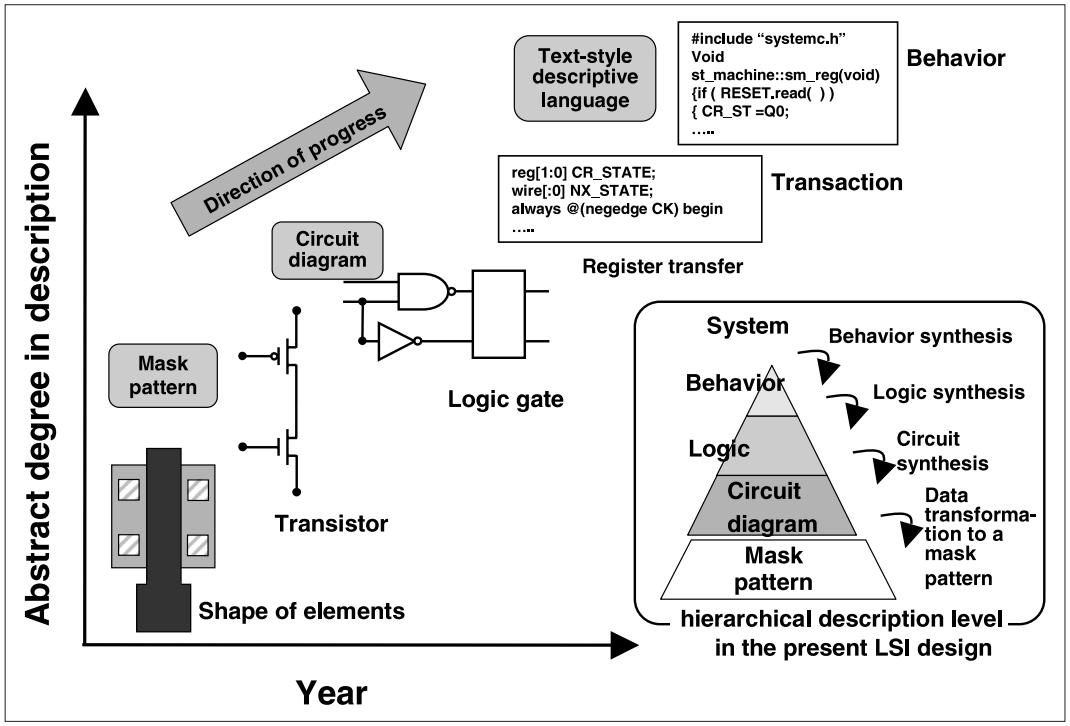
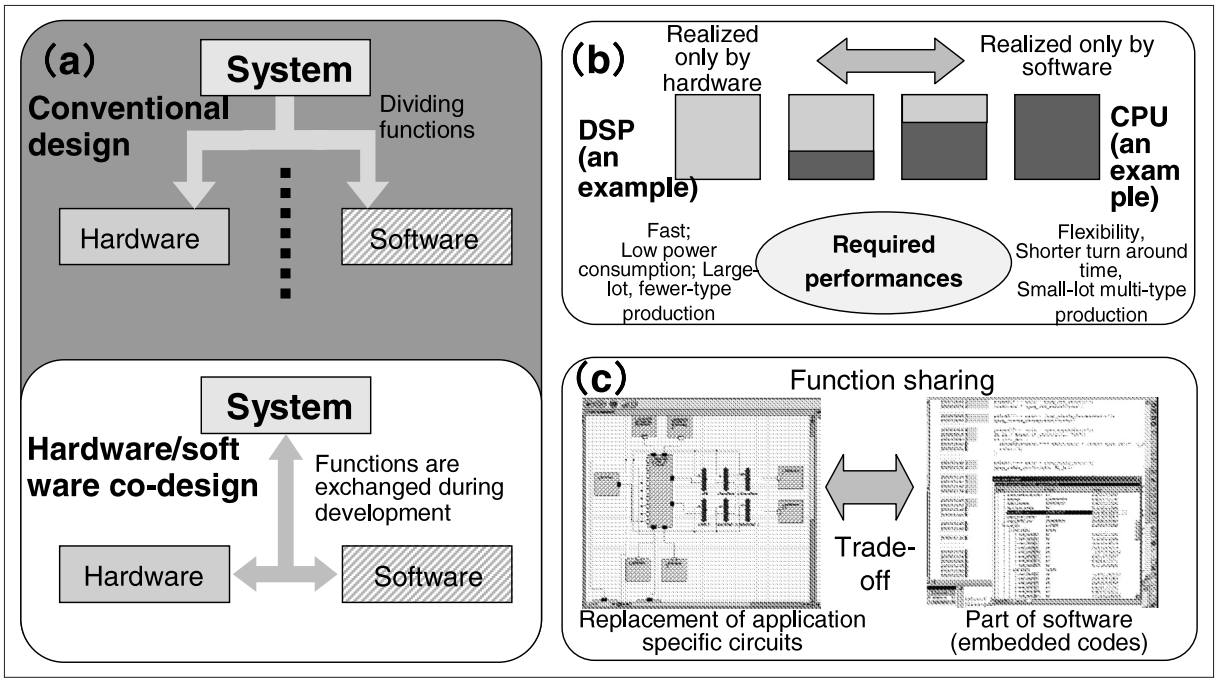


Figure 6 : Hardware/software co-design



is then used for mass production of products, due to its longer development period. Employing more software-dependent functions, the system becomes more flexible for development, and can then be used for products for a specific market, due to the shorter turn around time, as shown in Figure 6(b).

The hardware descriptive language, which has replaced symbol-based description, provides advantages during the hardware/software co-design process, whereby the development of hardware and software is smoothly linked from an initial rough-sketch of an LSI to a final system operational test. In the early 90s, LSI hardware was computer designed, and its operation was tested by a computerized logic simulation. Before the introduction of hardware/software co-design, an LSI was designed after dividing its functions into hard- and software related respectively.

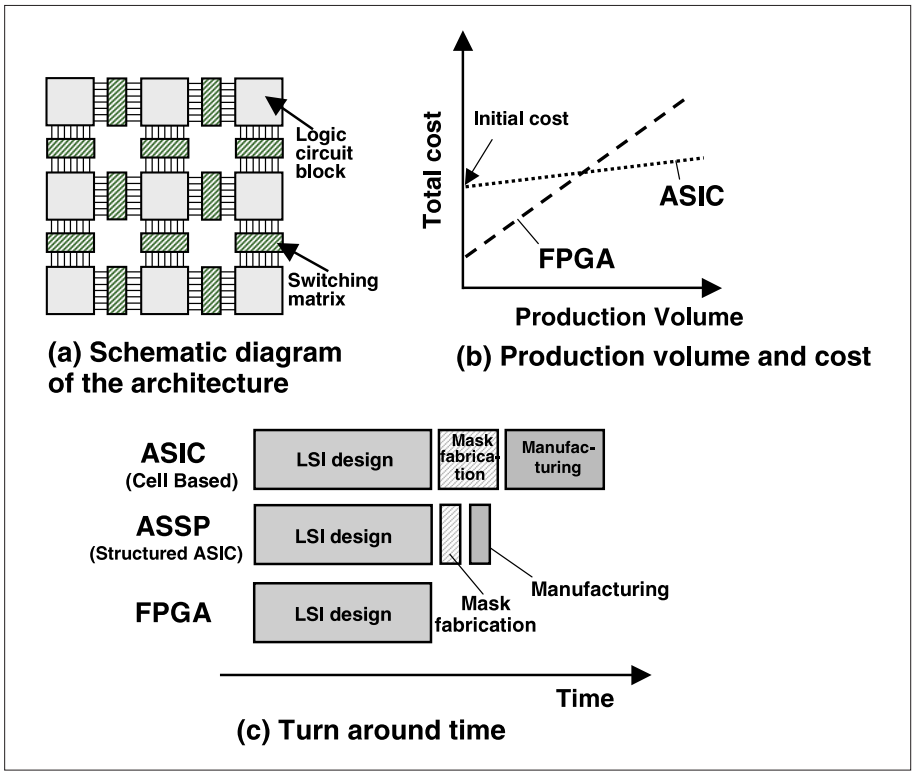
The hardware/software co-design has the advantage of a shorter turn around time, but prior to introduction, software was developed once the hardware specification was established, at a time when hardware and software could not be developed alongside each other in parallel. Given the advent of certain problems unable to be resolved through the use of software alone, hardware had to be re-designed, which considerably extended the period of time required for hardware development. However, hardware/software co-designs effectively prevented any such loss in turn around time.

(2) Shorter turn around time of LSIs

The aforementioned LSI design technology contributes, to some extent, to designing and commercializing increasingly highly-integrated LSIs in a shorter period, whereby another technology is attracting attention based on a tendency toward shorter product life-cycles. In conventional technology, LSIs are manufactured using masks prepared once designs are completed and are individually prepared for each product or customer respectively. A field programmable gate array (FPGA) and programmable logic device (PLD) contrast with the individual-mask manufacturing process, in which a customer realizes their desired functions by electrically arranging internal LSI connections, in which elements and connections are laid out in lattice form.

The FPGA is constructed by laying logic blocks and switching matrices in a lattice form, as shown in Figure 7(a). The FPGAs are manufactured using common masks, rather than those specific to a product or customer, and are used after electrically switching the internal connections through programming. The common mask reduces the initial cost to a level less than that required by an application specific integrated

Figure 7 : Shorter turn around time employing programmable LSIs



circuit (ASIC), as shown in Figure 7(b), and also shortens turn around time, contrasting with that required by individual-mask manufacturing, with a few months of manufacturing lead-time, as shown in Figure 7(c).

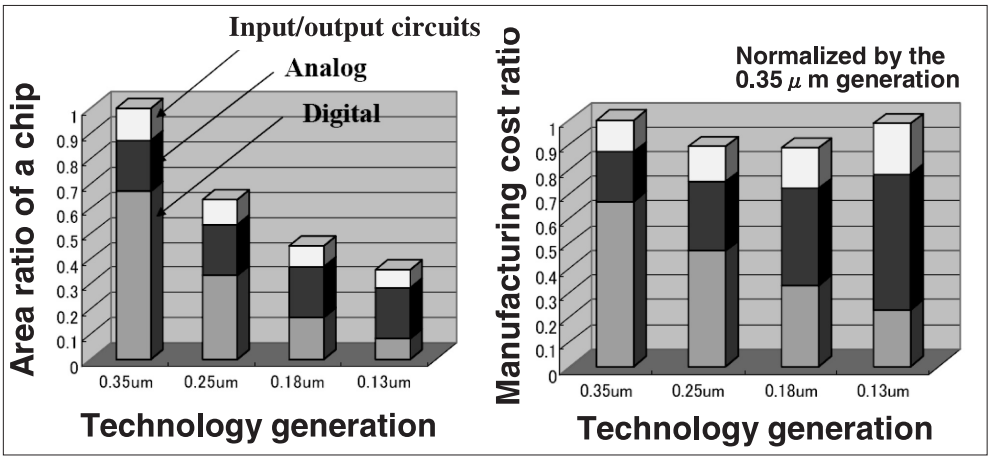
So far, the FPGA has encountered setbacks, such as the redundant use of logic circuits, reduced processing speed, and higher power consumption. The setbacks limited the use of FPGA only in test-production for function checks, etc, owing to disadvantages in integration, processing speed, power consumption, and price, in comparison with the same generation of LSIs. The FPGA was not commercially manufactured, and was replaced by LSIs for mass-production, where the FPGA-certified design was transferred to the LSI accompanied by certain reconfiguration of physical layouts, etc.

Despite the setbacks, the market requires the FPGA, under the present circumstances: The LSI manufacturing technology has seen LSI design progress ever further. This allows, in some cases, improved FPGA performance implementing the latest LSI manufacturing technology, although the FPGA remains hampered by the inclusion of redundant switching matrices. In addition, certain FPGAs are manufactured at a competitive cost in the case of small-batch manufacturing, due to the increasing cost of manufacturing LSIs: the increasing cost of mask fabrication (exceeding 100 million Yen for LSIs) and increasing risk (in terms of the development cost and period) of re-fabrication of the mask being required due to design failures. Demonstrating the remarkable progress of FPGA technology, Xilinx, Inc., U.S.A., has recently commercialized an FPGA product using a 90 nm process (power supply voltage: 1.5 V, multi-processor, large memory: a few Mb, system clock frequency: 500 MHz, equipped with clock management).

Recently, there has been considerable focus on application specific standard products (ASSPs), located midway between the ASIC and FPGA in terms of performance and cost. The lower layers of the wafer are common among certain ASSPs, while upper layers are customized for each customer. The ASSP has the advantage of basic functions being standardized, one example of which is a cellular phone ASSP standardized by a wireless telecommunication protocol. In this case, the ASSP is manufactured using IPs*1, namely, reusable circuit-design assets. An embedded processor is manufactured licensing IPs owned by ARM Ltd., UK, representing the de facto standard in this field.

ASIC is comprised of a “cell,” (the smallest ASIC

Figure 8 : Area ratio of analog circuits on an LSI chip and manufacturing cost



Source: Reference[5] by courtesy of Prof. Matsuzawa, Tokyo Institute of Technology

unit) that is developed by each manufacturer. This represents a "vertically integrated product," with which Japanese companies have considerable expertise and includes the advantage of large-lot, fewer-type production. Digital home appliances are, however, standardized in most signal interfaces, making it difficult to render superior performance. Each appliance is thus only allowed superiority in peripheral functions, etc.

(3) Increasing importance of Analog-circuit design technology

With the miniaturization of digital circuits and automated design of LSIs, the importance of analog circuits is increasing. Even when the signal processing is digitized, it is impossible to eliminate analog circuits, one reason for which is the fact that a digital signal is converted to a human-sensible analog through a human interface. A deteriorated digital signal is recovered using analog-circuit technology when a digital signal is disturbed or faded during the read/write of high-density data or broadband communication. Analog technology has long been believed to require considerable knowledge and experience on the part of design engineers, from the time when discrete components were assembled into circuits. The analog circuit, which handles small-amplitude high-frequency signals in many cases, requires a large number of circuit-property indicators than the digital equivalent. Together with knowledge on materials and physical qualities of elements, the analog circuit demands on the part of design engineers for a broad range of knowledge on a system in order to totally optimize it.

The elements of a digital circuit reduce in size according to the "scaling rule," and experience enhanced performance over the course of a new generation of technological change, while analog elements include a variety of passive elements*2 and are only miniaturized to a limited extent over the course of the technological generation change: for example, there is a trade-off between the respective miniaturization and high-performance of inductors. The analog circuits start expanding surface areas in comparison with shrinking digital circuits, which has an increasing influence on the LSI manufacturing cost, as shown in Figure 8. The design period of the analog circuit is relatively longer, due to a lack of design automation tools and the design adjustment required to maximize the performance of the heavily-manufacturing-de pendent analog circuit.

The design and manufacturing cost of LSIs is becoming dependent on the analog circuit, while a cellular phone, a representative product using high-frequency analog LSIs, is renewed every few months. The analog circuit will play an important role in reducing development and manufacturing costs and commercialization of competitive products, where the analog circuit may suffer from a lack of design engineers owing to the longer period of time required to educate such engineers.

(4) Future trends

The design technology is facing a crisis

due to its slow progress in comparison with manufacturing, particularly in terms of productivity, as discussed in Chapter 1. Testing technologies of design and products are also inferior to actual design technology, a situation predicted to worsen as LSI development becomes more sophisticated to meet a variety of requirements. However, this is a region where an innovative technology may arise.

On the other hand, LSI design technology and manufacturing have become mutually dependent, where new methodologies such as design for manufacturing (DFM) and design for yield (DFY)[6] have been proposed. Although the LSI yield had been believed to be governed by manufacturing technology, a couple of reports claim that design technology governs the yield more than that of manufacturing following the technology generation of 90 nm.

The design technology is understood as becoming more important to bridge increasing ly-sophisticated manufacturing technology and a system which will demand more various and more complicated performances. Progress in LSI and LSI applications (electronic appliances) may not be achieved without equivalent progress in LSI design technology.

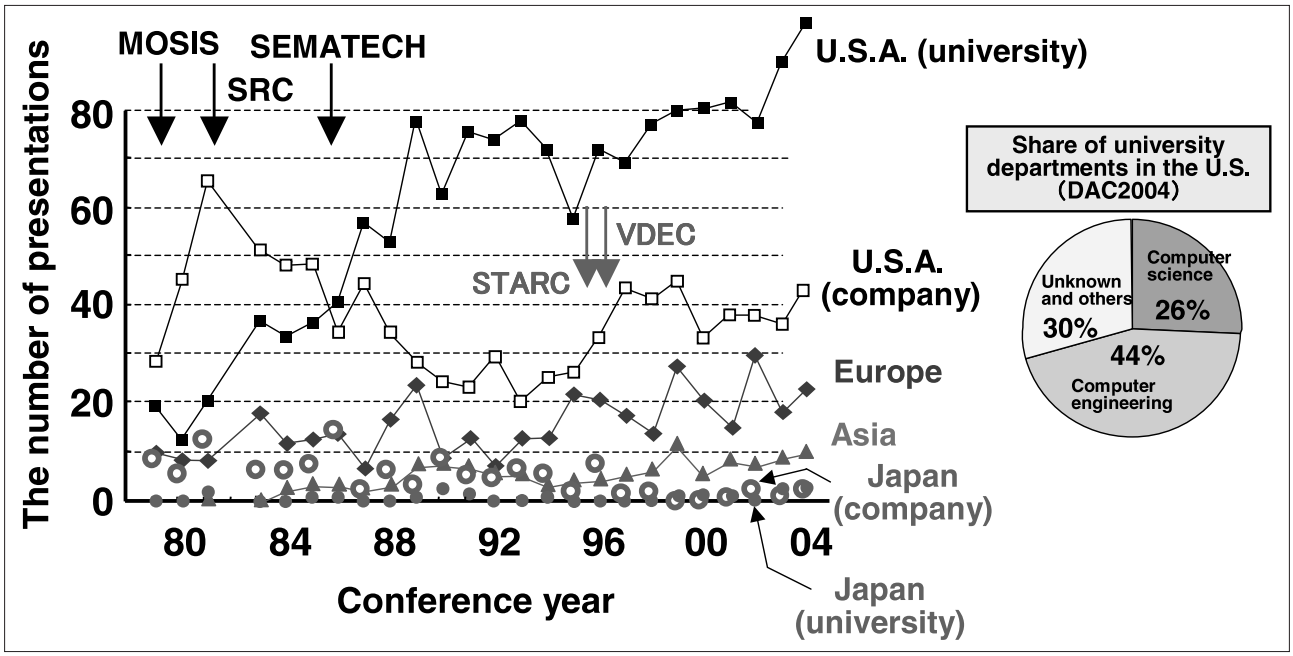
3 Present R&D status and its issues

3-1 In view of the number of presentations at conference and filed patents

Figure 9 shows trends in the number of presentations at Design Automation Conference (DAC), one of the most prestigious LSI design conference[7].

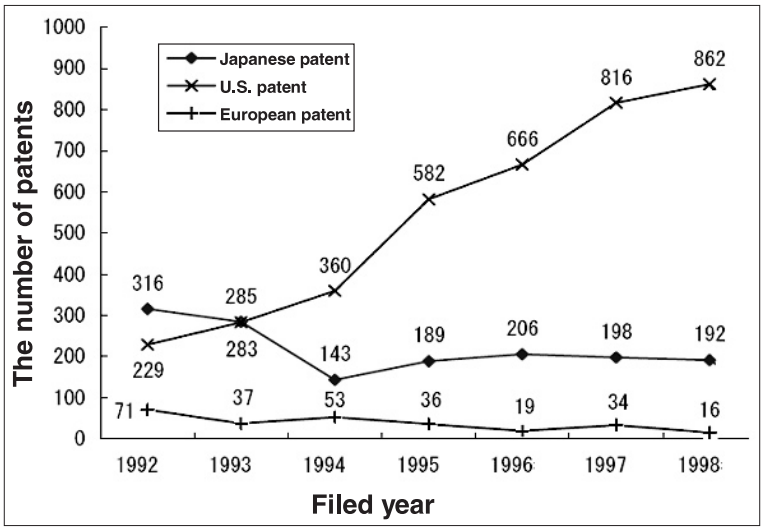
In the early 80s, U.S. companies shared most of the presentations. Once a test-production service had started at the MOSIS, U.S.A., an institution funded by the government, and the industry-university collaboration at the Semiconductor Research Corporation (SRC) got underway, presentation by U.S. universities increased greatly. Presentations from Japan, however, mainly by Japanese companies, numbered about 10 in the early 80s, comparable to that from Europe (including both companies and universities). Post 80s, however, Europe gradually increased the number of presentations, while Japan decreased its volume to 2 or 3 in the 1990s and shows no sign of advancing on this figure at present. In Japan, despite the existence of the VLSI Design and Education Center (VDEC), an LSI test-production institution comparable to the MOSIS, and the Semiconductor Technology

Figure 9 : The number of presentations at DAC by country/area and university/company



Source: The graph of "The number of presentations," courtesy of Dr. kozawa, STARC.

Figure 10 : The number of EDA patents filed in Japan, Europe, and U.S.A.



Source: Reference[8]

Academic Research Center (STARC), funded by business, which have been in operation since the mid 1990s, publications from Japanese universities, which have been scarce to date, show no signs of any increase up to now.

Dividing the number of presentations from the U.S. and Japan into companies and universities respectively, the figures are plotted on Figure 9, where presentations from Europe and Asia (excluding Japan) are mainly contributed by universities [note1]. As shown in the circle graph in Figure 9, 70% of the presentations at DAC 2004 were contributed by computer-related departments.

Patent numbers filed in Japan, Europe, and the U.S. are summarized in Figure 10. In the early 90s, many Japanese patents were filed mainly by Japanese companies, indicating that design technology was developed to some extent by Japanese companies at that time. However, U.S. patent filing increased far more than Japanese patents in the 90s.

To date, Japanese companies have conducted vertically-integrated semiconductor businesses, where LSI design tools and IPs were developed in house, coupled with design methodology development. Recently, however, Japanese companies have tended to replace self-developed tools and IPs with de facto standard EDA tools and IPs provided by U.S. vendors, considering the productivity of development and maintenance. The small number of presentations by Japanese companies may also reflect this trend. Japanese companies are moving toward users of tools and IPs, without research into the associated methodology.

One reason why Japanese companies are behind the recent progress in design technology is related to their success in semiconductor memory manufacturing. Memory design and manufacture in this area are not as complicated as with functional LSIs: the increase of elements in memory is accomplished without further design complication, despite an exponential increase in elements. The U.S. companies shifted their business from memory chips to functional LSIs, once the memory manufacturing business shifted from the U.S. to Japan in the late 80s. Realizing the importance of LSI design technology, U.S. companies strategically conducted their R&D on design technology, while Japanese companies may require considerable time to gain a competitive edge in this technology.

Note

1 The share of presentation at DAC 2004. Companies in Europe, 2%; universities in Europe, 12%; companies in Asia (besides Japan), 0.8%; universities in Asia (besides Japan), 10.2%.

3-2 R&D promoting activities in some countries

R&D on LSI design technology is promoted in certain countries[9, 10], as shown in Table

2. Taiwan, in particular, has been attracting attention for its promotional program in this field. Following the success of its foundry business, Taiwan is trying to renovate its industry structure from manufacturing to LSI design, assisted by government promotion. The LSI design technology, as a successfully highly-prioritized field, has been reinforced in a short period. The Si-Soft project[11], started in 2003, targets the reinforcement of design technology and involves more than 255 professors and associate professors being invited, mainly from the U.S., over 3 years, and the investment of 100 billion Yen over 4 years: of which 30% is from government and 70% from companies.

In the U.S., the federal government has funded design research in universities from the early phase of this technology, promoting

Table 2 : Research promoting activities in countries and areas

Region	Government project, etc	Major participants	Budget	Remarks
U.S.A.	FCRP backed by MOSIS, SRC, and MARCO(from 1998), etc. Design, test, and interconnection technologies in universities are reinforced.	UCB, University of Illinois, CMU, Stanford University, University of Texas, many others	SRC: budget, about 4.5 billion Yen a year; FCRP: 1 billion Yen a year.	Private companies (EDA tool vendors, Intel, IBM, etc.) develop the design technology, as well. A private organization is standardizing the interface, etc.
Europe	The organization on information and communication technologies in the European Commission prioritizes the reinforcement of semiconductor technology, with an industry-government-university collaboration under way: Alba (Scotland), IMEC (Belgium), and LETI (France).	STM, local universities, many others	IMEC: budget, 10 billion Yen a year; Alba: budget, 10 billion Yen a year (Semiconductor)	Serious in educating on design technology; Europe is competitive in analog communication ASICs for Nokia, etc.
Taiwan	The Si-Soft project is under way (from 2003, 4 years). Taiwan plans to double the number of university researchers, inviting more than 255 professors and associate professors in 3 years from overseas (mainly from the U.S.A.). More than 1,000 design engineers and researchers (Masters and PhD.) a year are planned to be produced by this increase.	National Taiwan University, National Tsuing Hua University, National Chiao-Tong University, National Cheng-Kung University	Si-Soft project: budget, 100 billion Yen for 4 years	The government reinforces industry design technology, and renovates the industrial structure.
South Korea	The Embedded System Research Center (ESRC) was established in ISRC. Research into embedded system software, SoC design technology, and real-time OS.	KAIST, Seoul National University, ISRC (ESRC)	ISRC: budget, about 1.5 billion Yen a year.	Samsung announced a focus on system LSIs henceforth.
China	Government has assigned seven areas (Shanghai, Beijing, Wuxi, Chengdu, Dalian, etc.) for their IC industry development. There is the government funded IC R&D Center (test-production, EDA, product-test service), in which universities have established a number of design-related venture companies.	Tsinghua University, Shanghai Jiao Tong University, Beijing University, Fudan University, Dalian University of Technology		China is planning to standardize its own EDA.
Japan	Reinforcing the design capability at VDEC and STARC. Promoted by the Fukuoka Pref. System LSI Designing Base Development Project (started in 2001) and the Kyushu Silicon Cluster Formation Program (Council of Silicon Innovation, Kyushu).	Kyushu University, Kyushu Institute of Technology, Fukuoka University, Waseda University, etc, STARC	VDEC: budget, about 400 million Yen a year; STARC: capital, 440 million Yen; Fukuoka IST: budget, 2,560 million Yen	In operation in the Kyushu region, etc., funded mainly by local governments.

MOSIS: Institute for the test-production of LSIs, built by the government and privatized shortly afterwards.
SRC: Semiconductor Research Corporation: Established in 1982 with the objective that the universities conduct research to meet the needs of participating companies.
FCRP: The Focus Center Research Program: A project to reinforce research into non-competitive, commonly-shared technology by U.S. universities.
IMEC: Inter-University Microelectronics Center: Started in 1984 as a non-profit organization, currently employing over 1,000 researchers.
ISRC: Inter-university Semiconductor Research Center: Established in 1985 with the objective of promoting industry-government-univers ity collaboration.
VDEC: VLSI Design and Education Center: Design education center for large-scale systems. An institute to support universities for their education on LSI design and test-production.
STARC: Semiconductor Technology Academic Research Center: Institute to support industry-university collaboration funded by companies.
Source: Prepared by the authors, based on references[9, 10]

the establishment of venture companies, some of which have influential R&D power in this field. Besides venture companies, Intel, IBM, etc. have been developing EDA tools and design methodology to develop state-of-the-art LSIs.

In Europe, LSI design technology has been reinforced by industry-university collaboration, such as that in the Inter-university of the MicroElectronics Center (IMEC) from the early phase of technology under the initiative of the European Commission. STMicroelectronics, IMEC, etc. show their strength in high-frequency analog LSIs for wireless communication, having Nokia (a world-beating cellular phone manufacturer) as a customer.

In South Korea, a government-funded design-technology development project was started in February 2005 and is focusing on embedded systems. This project targets the reinforcement of technology for embedded software and systems.

Together with reinforcing LSI design technology, China is promoting R&D in LSI design methodology, backed by its huge market. Using the EDA tools currently provided by U.S. companies, China is attempting to develop its own proprietary EDA tools to replace the U.S. tools.

In Japan, VDEC (government project) and STARC (industry-university collaboration) have been in operation for about 10 years, although their budgets are uncompetitive. Recently, a project to develop the LSI design technology got underway in Fukuoka prefecture, promoted by local government. However, except for projects funded by local governments and companies, there is no project well funded by national government.

Following the success of the Semiconductor Manufacturing Technology (SEMATECH)[*3], common interfaces are proposed to effectively exploit design environments and IPs, which are monopolized and solely provided by the U.S. They are, for example, the Virtual Socket Interface Alliance (VSIA, established in 1996) and the Structure for Packaging, Integrating, and Re-using IP within Tool-flows (SPIRIT, established in 2003).

SEMATECH standardized interfaces are used within semiconductor manufacturing equipment as a form of non-competitive commonly-shared technology, which has enabled the flexible combination of equipment within a manufacturing factory. This has promoted the use of standardized, de facto equipment for specialized manufacturers.

4 To strengthen competitive technologies

4-1 Why LSI design methodology ?

The EDA tool industry is one of the smallest segments in the semiconductor business, sharing about 400 billion Yen (2% of the semiconductor market). The productivity of LSI design is dependent on the performance of such EDA tools, which therefore play an important role in overall industry progress.

Semiconductor manufacturing technology in Japan was believed to have a cutting edge, particularly in terms of DRAM manufacturing. When the interfaces between manufacturing equipment were standardized by SEMATECH, this opened the way for specialized manufacturing, opening the door to the innovative manufacture of LSIs and allowing any company in possession of de facto equipment to do so. The technology materialized in the form of equipment, where Japanese companies, with competitiveness in the shape of combined technologies, lost their competitiveness. Japanese companies did not have competitiveness in terms of equipment, while other equipment vendors provide their standardized products to a global market, ensuring a uniform level of quality in manufacturing technology worldwide. Under such circumstances, the LSI manufacturing companies, unable to develop their technical advantages, face difficulties in establishing barriers to entry.

The LSI design has been developed in the same way as DRAM manufacturing technology, where the enhancement of design productivity has allowed the introduction of IPs in the form of IP-based design or platform design[*4], to become increasingly commercially available. With progress in interface standardization by institutes and companies discussed in

Chapter 3, the LSI design is specialized in individual fields, dividing providers and users of the design tools. Every design engineer can complete their job with quality, provided the engineers have highly-automated tools and commercially-available IPs, meaning differences in engineer quality and certain improvements to tools do not affect the final product. However, the personnel cost may govern the competitiveness of the LSI design.

The imported EDA tools and IPs may jeopardize national industrial security: thus their export regulation puts a stop to the LSI design, even when the LSI manufacturing industry competes effectively on a global scale. In addition to industrial competitiveness, certain key components used inside the country should avoid excessive dependence on imported design tools. Considering this risk, China is attempting to develop its own design methodology and form of EDA technology, possibly also providing its own standard of tools.

A value-added LSI design is substantially governed by LSI design methodology, used to develop commercial IPs and common design tools. Without knowledge and expertise concerning this methodology, the limits and issues of the present methodology cannot be understood, and people remain incapable of coping with newly-emerging problems. Competitive LSI design technology is recognized as technology used to produce and move to the next-generation design methodology.

4-2 Action in scope

The LSI design technology of Japan (mainly Japanese companies) was more competitive than the present, as discussed in previous chapters. The competitiveness in the R&D of Japanese companies has been lost, while that of Japanese universities shows no progression. Recently, countries and certain regions in Asia, other than Japan, have been promoting development of LSI design technology to achieve reinforcement in a short period of time.

Considering current circumstances, actions are proposed to a certain extent to reinforce the competitiveness of LSI design technology in Japan.

It is vital to retain a number of engineers and researchers, and properly educate them, as innovative design technology develops; incorporating new ideas and fresh capability to materialize the latter, fully dependent on the ability of engineers and researchers. Researchers in silicon LSI technology are extremely lacking in Japanese universities, in comparison with other countries [note2]. Certain tertiary research programs also failed to keep pace with the change in the semiconductor industry structure. Research into III-V column compound semiconductors, such as GaAs, represents 25% of the programs in universities in Japan, though the share for compound semiconductors is as small as 1 to 2% of semiconductor sales[12], representing a smaller number of Si-related researchers in Japanese universities than that overseas. The inclusion of some industry and overseas researchers should be considered in Japanese universities, to compensate for this mismatch.

In the long run, education on design technology should be reinforced in Japanese universities. The contribution by computer-related departments in universities is remarkable in the U.S. (Figure 9), Europe, and Asian countries apart from Japan, meaning certain measures to reinforce related areas of education in Japanese universities are highly anticipated[12, 13].

When a new LSI is designed, the development of a new methodology is also often necessary.

Together with each government-funded program for design methodology used to develop key LSIs, one of the actions involves conducting a government project, for example, focusing on security-related LSI technology as one of the basic technologies of the ubiquitous network.

This new LSI technology is related to that used to establish secure environments in the fields of electronic currency, identity recognition,

Note

2 This field in Japanese universities is comprised of 50 professors and vice professors. The Si-Soft project in Taiwan is planning to, at least, double the number of researchers (at 200 before the project) in universities in three years

and encryption. The new-LSI development will contribute to reinforcing Japan-original LSI design technology, even if the LSI is not highly integrated and may not share a large market in the semiconductor business. LSI design relating to national security should not be dependent on the "black-box" imported EDA tools and IPs. In addition, a synergistical technical effect is expected when the new LSI design methodology is successfully developed.

Well-experienced engineers, who were in charge of the development of EDA technology in Japanese companies, still have the capability to work. They may contribute toward reinforcing EDA technology in Japan, collaborating with younger engineers and transferring their expertise. If the present chance is lost, the engineers teaching LSI design technology may become too senior and be lost, thus prompting an influx of overseas design engineers, together with EDA tools. It is the last chance for their expertise to be transferred to and maximized in the younger generation.

LSI design technology will face future issues, which may arise in analog circuit design, and design and product testing. Besides those, a variety of issues may arise in the increasingly-sophisticated LSIs. In the field of consumer electronic appliances, the most advanced and sophisticated LSIs are, however, commercialized in Japan prior to other countries and areas. Japan has a market with the advantage of accepting advanced and innovative systems and LSI design. The highly-valued requirements for LSIs should not be presented only to foreign EDA tool vendors from LSI manufacturers in Japan, which are encouraged to share technical issues with universities through conferences, exhibitions, and industry-university communication. Sufficient technical capability to resolve current issues is demanded on the part of universities.

5 Conclusions

The value of electronic appliances is becoming governed by system LSIs, where shortening appliance life cycles are rendering technology to design sophisticated LSIs in a short period vital. LSI development is more heavily dependent on design technology rather than manufacturing, and is facing a bottle-neck in such design technology.

LSI design methodology has shown progress each decade, abstracting the design description method: in the 70s, the layout pattern of elements; in the 80s, circuit diagrams using symbols; and in the 90s, text-style language. The design technology has progressed alongside software technology development.

Design technology in Japan, however, which was behind the progress of the highly abstracted description, has not shown equivalent progress, since the description has become more highly abstract. The presentation of design research by companies, universities, and institutions in Japan, has actually gone down at DAC, a prestigious conference in this field, where accepted presentations from Japan currently represent 2% of the whole.

Universities share 70% of DAC presentations, and play an important role in developing design technology. U.S. universities began to increase the number of presentations accepted at DAC once the LSI test-production service and industry-academy collaboration got underway. Taiwan, meanwhile, successful in semiconductor manufacturing, has been rapidly reinforcing their LSI design technology, under government leadership. With other regions and countries also reinforcing such technology, Japan is being left behind.

More researchers in this field, where a lack of numbers causes R&D to deteriorate, are necessary in Japan. In the short run, researchers may be employed from industry or foreign countries, but in the longer term, the university education related to computer science or engineering should be reinforced to produce engineers and researchers capable of developing design technology.

A new LSI design methodology could then be developed, powered by the competitiveness of the design technology, and should progress through the development of nationally essential LSIs, such as those security-related.

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Glossary

*1 IP
Stands for "intellectual property," and, in the field of semiconductors, represents a design asset related to circuits or devices, distributed for re-use.

*2 A passive element
An element incapable of amplifying input signal power. Its property is, in many cases, governed by its physical shape or the material used.

*3 SEMATECH
Stands for "SEmiconductor MAnufacturing TECHnology," and is a consortium co-funded by the Department of Defense, U.S.A., and four private semiconductor manufacturers, in which the semiconductor manufacturing technology is studied. This was established to recover the U.S. semiconductor industry that had lost its way in the 80s.

*4 IP-based design
platform design. A method used to design system LSIs, where virtual components (VCs) and virtual sockets (VSs) are used, as a print circuit board is designed and developed: one IP (design asset , such as functional modules) makes up a VC, and different kinds of IPs are combined using VSs. Standardized interfaces between IPs facilitate their commercial use.

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